BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

(19) Europäisch s Patentamt
Eur pean Pat nt Office
Office europé n des brevets

(11) Publication number: **0 592 783 A2**

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: **93112569.4**

(51) Int. Cl.5: **G06F 1/08**

(22) Date of filing: **05.08.93**

(30) Priority: **16.10.92 US 962437**

(43) Date of publication of application:
20.04.94 Bulletin 94/16

(84) Designated Contracting States:
AT BE CH DE DK ES FR GB GR IE IT LI LU MC NL PT SE

(71) Applicant: **PICOPOWER TECHNOLOGY INC.**
1975 Concourse Drive
San Jose, California 95131(US)

(72) Inventor: **Kenny, John D.**
1017 Rosa Avenue
Sunnyvale, California 94086(US)
Inventor: **Lei, Emilia V.**
33 Union Square, Apt. 732
Union City, California 94587(US)

(74) Representative: **Polus, Camille et al**
c/o Cabinet Lavoix
2, Place d'Estienne d'Orves
F-75441 Paris Cedex 09 (FR)

(54) Heat regulator for integrated circuits.

(57) The temperature of a circuit is monitored and controlled by accumulating an estimate of heat generated in the circuit, and decreasing heat generation in the circuit when necessary. A periodic sampling of the operating mode of the circuit, as determined by clock speed and bus cycle activity, is used to determine heat accumulation in the circuit. An up/down counter increments when the sampling shows an operating mode indicating heating of the circuit and decrements when the sampled mode indicates cooling of the circuit. The circuit is forced to cool if a count on the up/down counter reaches a programmable threshold. Cooling is accomplished by slowing the clock speed of the circuit.

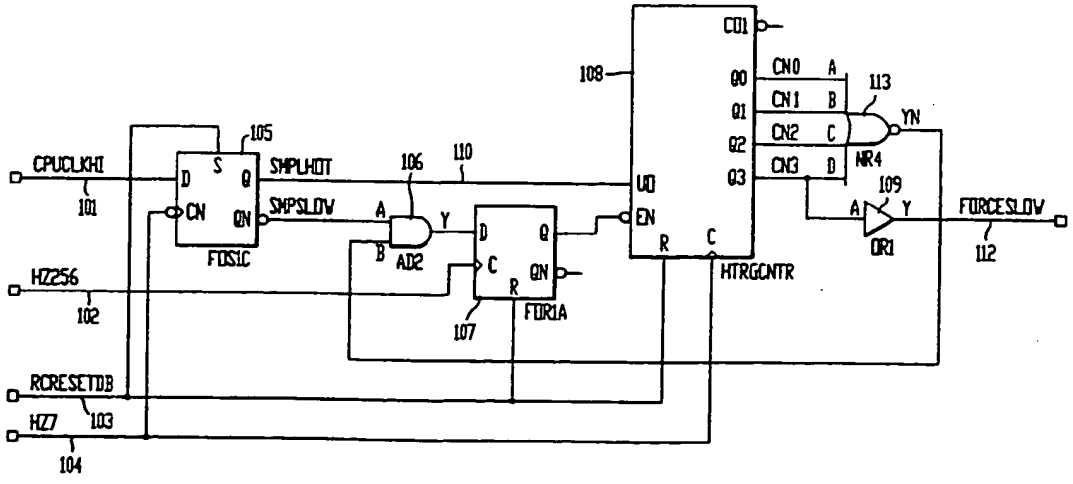

FIG. 1

EP 0 592 783 A2

integrated circuit is generating too much heat and its temperature is increasing. The temperature count is correspondingly increased. When the sampling indicates a low frequency, this indicates that the integrated circuit's temperature is either cool or cooling, such that the temperature count is thereby decreased.

This method of monitoring and regulating temperature in an integrated circuit works because the heat generation in an integrated circuit is proportional to current flow, and current flow in a CMOS integrated circuit is directly proportional to the switching frequency of the circuit, commonly known as clock frequency. This indicates that heat generation is itself proportional to clock frequency.

Another embodiment of the invention includes the enhancement of monitoring the effective clock frequency of the external bus cycles in addition to the previously described scheme of monitoring only the core system clock. In many integrated circuits there are two significant parts of the circuit that operate at different frequencies. Generally there is a main system clock that clocks internal circuitry and there is a separate clock, or similar control mechanism, that clocks the output buffers of the integrated circuit. The current flow, and resultant heat generation, produced by the output buffers can be very large due to the fact that current flow is also directly proportional to load capacitance and output buffers typically drive significant capacitive loads. The specific equation defining this relationship is, $I = CV^2F$. Where I is current, C is capacitance, and F is frequency.

In a typical CMOS CPU it can be shown that the clock frequency of the internal circuitry accounts for approximately two thirds of the total current flow, whereas the effective clock frequency of the output buffers accounts for approximately one third of the total. If both factors are monitored simultaneously and the two factors are averaged in a weighted two to one ratio, an accurate assessment of the circuit's total current flow can be determined.

The output bus of a CPU is not driven by a fixed frequency clock. Instead the effective clock rate is determined by how frequently external bus cycles occur. In most computing systems the occurrence rate of bus cycles varies constantly depending upon what type of instructions the system software chooses to execute.

The effective clock frequency of the output bus can be determined, however, by randomly sampling external bus activity. Since each specific CPU type has a maximum possible frequency for its external bus cycles, the effective clock frequency can be estimated in proportion to the maximum. For instance, if a particular CPU has a maximum bus cycl frequency of 8 MHz, this equates to a maximum of one cycle every 125 nS. The present invention would then trigger a BUS ACTIVE signal for 125 nS immediately following the start of very bus cycle. This signal would remain high for 125 nS following the start of every bus cycle. After 125 nS the BUS ACTIVE signal would drop to low, unless a new bus cycle started. The BUS ACTIVE signal would then be sampled on a periodic basis. If the BUS ACTIVE signal is always found to be high, then there must be one bus cycle occurring every 125 nS in order to keep the BUS ACTIVE signal high, and this indicates a bus speed of 8 MHz. But if, for instance, only half of the BUS ACTIVE samples are found to be high, it can th n be assumed that the effective bus clock frequency is only half of its maximum frequency or 4 MHz.

On a short term basis this type of periodic sampling could produce significant errors, but since the heat regulator's up/down counter averages large numbers of samples, and sinc th occurrence rate is a random phenomenon, the averaged result will be very accurate.

The up/down counter acts as both an averaging circuit and as a time delay element. Because the heat buildup in an integrated circuit is a relatively slow process, taking several minutes to reach its maximum heat, it is possible to allow the circuit to remain in a high heat generating state for several minutes before engaging active regulation to reduce the heat buildup. This delay is desirable because the heat regulator reduces heat by reducing the CPU's clock frequency which also has the undesirable effect of reducing system performance. It is preferable to delay active regulation until it is truly needed. This is achieved in the present invention by providing a programmable range of regulation delays.

Fortunately, this delay prevents the heat regulator from reducing performance under normal operating conditions, since normal operating conditions generally do not require that the CPU remain in a high heat generating state for more than a short period of time. In a typical computing system, short bursts of peak activity are separated by longer periods of relative inactivity. But since a computer system designer must design to the worst case scenario, the heat regulator becomes a very effective means of reducing the worst case heat condition without reducing system performance under normal operating conditions.

Another programmable variable provided for in the present invention is the power use ratio. In general, the power use ratio can be set at any value desired by varying the rate at which the counter counts up for a "hot" sample or the rate at which the counter counts down for a "cool" sample. In the embodim nt described below, the power use ratio is programmed to one of several options

when the CPU is running fast (such as 33 Mhz), and "cool" or zero when the CPU is running slow (such as 1 Mhz). Naturally the logic employ d could be reversed if desired so long as the remaining circuitry is adapted to work with the logic employed. The status line 101 is coupled to the data input of a D flip-flop 105. Flip-flop 105 samples the status line 101 at periodic intervals dependent on a timing signal 104 so that an output signal on lead 110 from flip-flop 105 indicates if the CPU was "hot" or "cool" when sampled.

The "hot" and "cool" signals are accumulated and averaged through an up/down counter 108. A counter clock signal on line 104 controls the rate at which counter 108 increments or decrements. In the circuit of figure 1, counter 108 increments or decrements once for every sampling of the CPU speed.

If counter 108 increments more than it decrements, the count in counter 108 will reach a threshold value. This threshold value will trigger temperature regulation by generating a signal on output line 112. The threshold value is set to a binary 1000 or a decimal 8. Whenever this threshold is reached, the output signal on lead 112 forces the CPU clock speed to slow. The slowing of the CPU clock causes a "cool" signal to appear on line 110 so counter 108 decrements during the next sampling interval. The CPU could then run "hot" in the following sampling interval causing counter 108 to count up to the threshold again and again generate a signal on lead 112 which forces the CPU to run slow again. In this manner after the threshold value is reached, the embodiment of the invention in Figure 1 maintains no more than one time interval of CPU running "hot" for every interval of CPU running "cool." The ratio of time running "hot" to time running "cool" is approximately equal to or less than one.

When the circuit continually samples the clock as "cool" the up/down counter will continue decrementing until it reaches a minimum value of zero. If the count reaches zero and the clock speed is again sampled as "cool" then the counter will be prevented from decrementing further by NOR gate 113, AND gate 106, and flip-flop 107 which detect the zero count and disable the counter until the next "hot" sampling of the CPU clock.

The average operating temperature of a circuit regulated by the embodiment of figure 1 can be determined by experiment. On way to determine the effect of the circuit in figure 1 on the operating temperature of the integrated circuit is to measure the equilibrium temperature of the integrated circuit when the integrated circuit operates at constant high clock, and measure the operating temperature when the integrated circuit operates at constant low clock speed, then time average the equilibrium temperatures.

The circuit of figure 1 causes the CPU to operate with a variabl op rating frequency, so the operating temperature of the circuit will not be constant but will fluctuate around an average temperature. The averaged temperature equals a tim average of the equilibrium temperatures for constant frequency operation, and is closely related to the power use ratio.

For example in a 486 system, when a CPU runs at 33 Mhz for a long period of time, the temperature of the CPU device might go up to 65 C in an open environment at room temperature where there is good air circulation. When the CPU runs at 1 MHz for a long time, the temperatur might only be 28 C in an open environment. If the system is running at 33 Mhz for one interval, at 1 Mhz for the next interval, at 33 Mhz for the next interval, and continues this pattern, then the temperature of the system fluctuates around av rag temperature (65 + 28)/2 C, i.e. 46.5 C, assuming the surroundings are at room temperature.

The circuit in figure 1 has a power use ratio of 50% and restricts the CPU operation to keep the ratio of time running at high speed operation to time running at low speed operation to less than approximately 1. Accordingly, the temperature difference between the CPU and the surroundings will be regulated as described above. Using the example data, if the CPU is in an environment at room temperature, then the operating temperature will be about 46.5 C.

The temperature of the integrated circuit can be somewhat higher than the average for a short period of time. For example, if the counter starts at zero with the CPU already at the desired average temperature, such as 46.5 C, the CPU can run at high speed for 8 timing cycles causing the temperature to rise temporarily above average regulation temperature. A certain temperature (such as 48 C) is reached. The actual temperature can be experimentally determined. During this time, the counter increments once each timing cycle and reaches the threshold of 8. The CPU is forced to low speed for a timing cycle, and the counter decrements to 7. The temperature can go no higher since from that point on for every interval of high speed operation there must be an interval of low speed operation. The temperature trends back to the average regulation temperature, even though the temperatur count remains near the threshold.

Figure 2 shows an embodiment of the present invention that monitors both the CPU clock speed and bus activity. In figure 2, the CPU clock status line 201 is multiplexed with a bus active line 221. For a typical operation, a bus select signal BUSACTVSEL on line 222 has a 33% duty cycle (1:2 high to low ratio), and has a frequ ncy that is on third

ing. The cooling forces the ratio of time spent at high speed to time spent at low speed back to two.

The average temp rature of the circuit can be calculated using the time average techniques described above. Using the example data, the average temperature should be (65 x 2 + 28 x 1)/3 C or about 52.7 C if the circuit is operating in a room temperature environment. The power use ratio and the average temperature changes if the select signal on lines 226 change. If for example the multiplexer 235 selected a signal HZ21 that had a frequency 3 time the incrementing frequency then the power use ration would be 75% and the average temperature would be (65 x 3 + 28 x 1)/4 C or about 54.8 C.

Figure 4 shows an embodiment of the invention generalized to the case where the circuit to be controlled has a number of operating modes. Among other possibilities, these different operating modes may include a number of different frequencies at which the circuit could operate or a number of different elements which generate heat that needs to be monitored.

In figure 4, the current operating mode of the circuit is indicated by signals on the status lines 401. The heat generation sensor 402 senses the signals on the status lines 401 and generates a sign signal on sign line 403 and a count clock signal on line 404. The two signals are dependent on the status signals and change periodically as the status lines 401 are sampled. The sign signal on line 403 has a value that indicates either that the circuit generates more heat than it loses or that the circuit loses more heat than it generates. The count clock signal on line 404 has a frequency that is proportional to the net heat change in the circuit when the circuit operates in the sampled operating mode.

An excess heat counter 405 keeps a temperature count of the net heat generated in the circuit. The counter 405 is connected to the sign line 403 and the count clock line 404 so that the counter 403 counts up or down depending on the signal on the sign line 403 by an amount dependent on the frequency of the signal on count clock line 404. The excess heat counter 405 outputs a count signal on lines 406 indicating the temperature count.

The cooling trigger 407 senses the count signal on the counter output lines 406. If the count reaches a programmable trigger value, the cooling trigger 407 generates a cooling activation signal on line 408. This signal forces the circuit to cool. One way to force the circuit to cool is to reduce the clock speed of the circuit. Of course other cooling means could also be triggered such as fans or refrigeration.

Anoth r embodiment of the inv ntion might utilize a contentional temperature monitor and a nov l power use regulator. Figure 5 shows a block diagram for such an embodiment. In figure 5, a temperature dependent resistor 501 would b mounted near the circuit to be monitored. When the temperature as indicated by a signal on line 505 reached a trigger value the power use regulator 502 would activate. The power use regulator might simply force the integrated circuit to low clock speed operation as long as the temperature is high. Instead the power use regulator could comprise the circuits of figures 2 or 3. The circuits would operate as long as the temperature monitor indicated high temperature, but would deactivate and reset wh n the temperature fell to an acceptable level.

Although the present invention has been d - scribed in detail, the description is only an illustration or example of the invention's application and should not be taken as a limitation. The scope of the present invention are limited only by the following claims.

Claims

1. An apparatus for regulating a temperature of a circuit operable in a plurality of modes, the apparatus comprising:
   (a) a temperature monitor; and
   (b) a power use regulator connected to the temperature monitor such that if the temperature monitor indicates temperature above a threshold value then the power use regulator limits a time that the circuit being regulated operates in modes which cause the temperature to rise above a desired value.

2. An apparatus for regulating a temperature of a circuit comprising:
   (a) a circuit activity monitor for providing a measure of the mode of operation of the circuit;
   (b) an excess heat counter coupled to the activity monitor for keeping a temperature count in response to the mode of operation of the circuit, the temperature count changing as a function of time at a rate selected to match net heat generation in the circuit at a desired temperature; and
   (c) a cooling trigger coupled to the excess heat counter, the cooling trigger causing the circuit to cool in response to the temperature count reaching a trigger value.

3. The apparatus of claim 2, wherein the cooling trigger comprises a device that sends a signal which forces the circuit being regulated to operate only in modes of operation which cause the circuit being regulated to cool toward a

(ii) a CPU clock speed status line which carries a signal indicating whether the CPU is currently running at the low clock speed or the high clock speed,

(iii) a set speed line for providing a control signal to the CPU to control the clock speed of the CPU, such that when a signal is asserted to the set speed line the CPU operates at the low speed,

(iv) a bus, and

(v) a bus activity line which carries a signal indicating the bus activity;

(b) the circuit activity monitor comprises:

(i) a multiplexer having a first signal input lead connected to the CPU clock status line, a second signal input lead connected to the bus activity line, a select input lead connectable a bus select timing clock, and an output lead for providing an output signal, the output signal being either the signal on the CPU clock status line or the signal on the bus activity line; and

(ii) a flip-flop with a data input lead connected to the output lead of the multiplexer, a clock input lead connectable to a sampling clock, and an output lead carrying a heat signal indicating either heating or cooling where high CPU clock speed or bus activity indicates heating;

(c) the excess heat counter comprises

(i) means for generating a count clock signal, and

(ii) an up/down counter with a plurality of output leads that carry signals which represent the temperature count, an up/down input lead connected to the output lead on the flip-flop so that when the heat signal indicates heating the up/down counter changes the temperature count in one direction, and when the heat signal indicates cooling the temperature count changes in the opposite direction, and a clock input lead connected to the means for generating a count timing signal thereby allowing the means for generating a count timing signal to determine when the counter output changes and the rate of the counter output change; and

(d) the cooling trigger comprises a device with one or more input lead and an output lead, the one or more input leads of the device being connected to one or more of the plurality of output leads of the up/down count r, the output lead of the device being connected to the set speed lin of th circuit so that the device can send a signal on the set speed line to force the circuit to low clock speed operation when the temperature count reaches the trigger valu .

13. The apparatus of claim 12, wherein means for generating a count clock signal comprises:

a means for multiplexing clock signals having a plurality of input leads, a select lead, and an output lead, the plurality of input l ads being connectable to a plurality of clocks which generate clock signals on the plurality of input leads, the output lead of the multiplexing means being connected to the clock lead of the up/down counter and carrying the count clock signal, the count clock signal being equal to a signal on one of the input leads.

14. A method for operating an integrated circuit at a desired operating temperature comprising the steps of:

(a) determining temperatures of the integrated circuit that results when the circuit operates in various operating modes; and

(b) limiting the amount of time that the integrated circuit spends operating in modes that result in temperatures higher than the desired operating temperature.

15. The method of claim 14 wherein step (b) further comprises limiting a ratio of the time that the circuit operates in a mode that results in temperature higher than the desired operating temperature to the time the circuit spends operating in a mode that results in temperatures lower than the desired temperature so that the ratio is not greater than a predetermined ratio that results in the desired temperature.

16. A method for controlling a temperature of a circuit operable in a plurality of modes, the method comprising the steps of:

(a) monitoring the activity of the circuit by sampling the operating mode of the circuit;

(b) accumulating a temperature count by successive additions values proportional to the net heat that would be accumulated in the circuit if the circuit operated in the sampled operating mode at a desired temperature for the time between samplings, the value possibly being negative; and

(c) forcing the circuit to cool if the temperature count is equal to or greater than a trigger value.

17. Th method of claim 16 wherein the circuit is forced to cool by forcing th circuit to operate for a tim only in modes where the heat gen rated in the circuit is l ss than th heat lost to

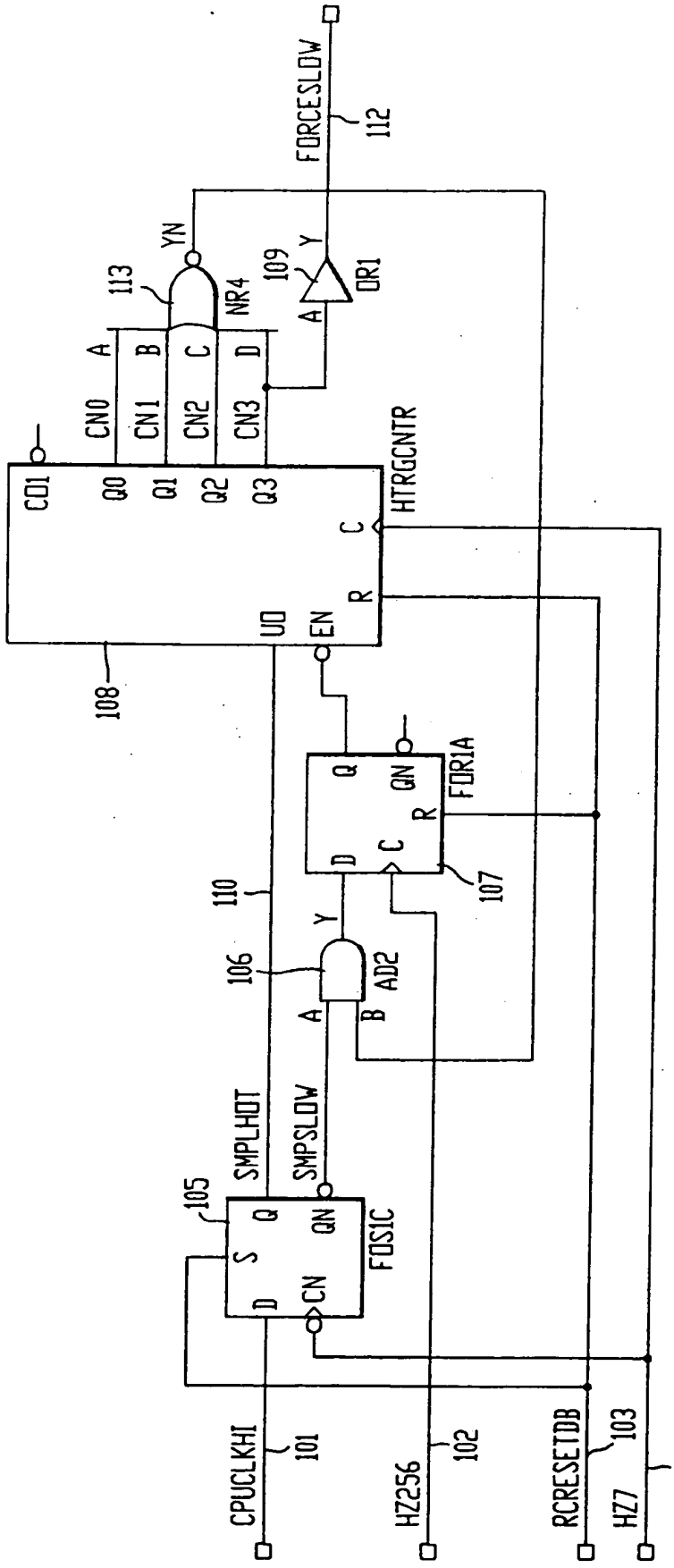
FORCESLOW
112
YN
113
NR4
109
Y
OR1
A
A
B
C
D
CN0
CN1
CN2
CN3
CO1
Q0
Q1
Q2
Q3
HTRGCNTR
C
R
UD
EN
108
Q
QN
FDRIA
R
D
C
107
110
Y
106
AD2
B
A
SMPLHOT
SMPSLOW
105
Q
S
QN
FDSIC
D
CN
CPUCLKHI
101
HZ256
102
RCRESETDB
103
HZ7
104

FIG. 1

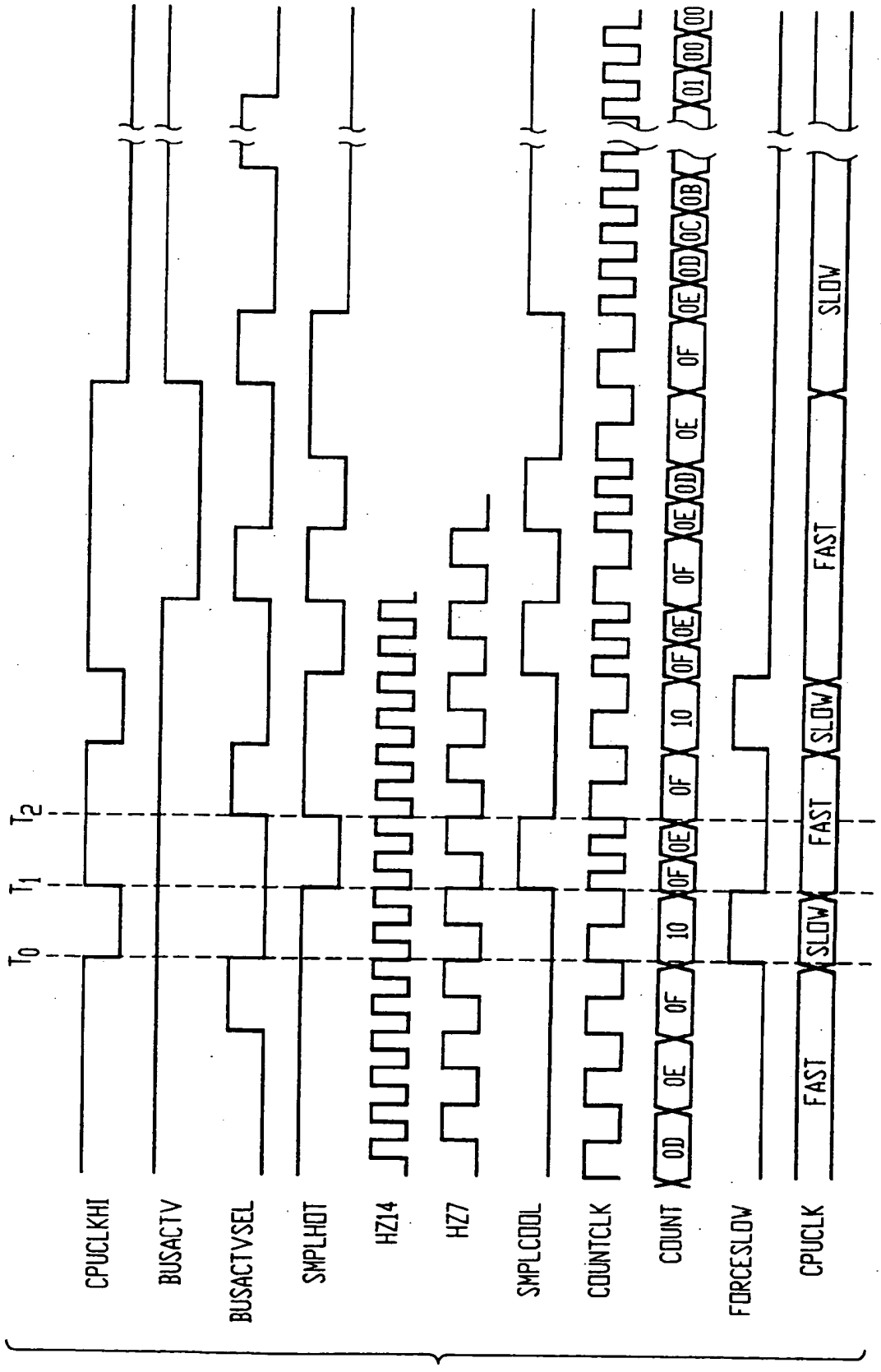
T0
T1
T2
CPUCLKHI
BUSACTV
BUSACTVSEL
SMPLHOT
HZ14
HZ7
SMPLCOOL
COUNTCLK
COUNT
FORCESLOW
CPUCLK
0D
0E
0F
10
FAST
SLOW
01
00
0B
0C

FIG. 3

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 592 783 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
24.01.1996 Bulletin 1996/04

(43) Date of publication A2:
20.04.1994 Bulletin 1994/16

(21) Application number: **93112569.4**

(22) Date of filing: **05.08.1993**

(51) Int. Cl.[6]: **G06F 1/08**, G06F 1/20, H02H 6/00

(84) Designated Contracting States:
AT BE CH DE DK ES FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **16.10.1992 US 962437**

(71) Applicant: **CIRRUS LOGIC, INC.**
Fremont, California 94538 (US)

(72) Inventors:
- **Kenny, John D.**
  Sunnyvale, California 94086 (US)
- **Lei, Emilia V.**
  Union City, California 94587 (US)

(74) Representative: **Polus, Camille et al**
F-75441 Paris Cedex 09 (FR)

(54) Heat regulator for integrated circuits

(57) The temperature of a circuit is monitored and controlled by accumulating an estimate of heat generated in the circuit, and decreasing heat generation in the circuit when necessary. A periodic sampling of the operating mode of the circuit, as determined by clock speed and bus cycle activity, is used to determine heat accumulation in the circuit. An up/down counter increments when the sampling shows an operating mode indicating heating of the circuit and decrements when the sampled mode indicates cooling of the circuit. The circuit is forced to cool if a count on the up/down counter reaches a programmable threshold. Cooling is accomplished by slowing the clock speed of the circuit.

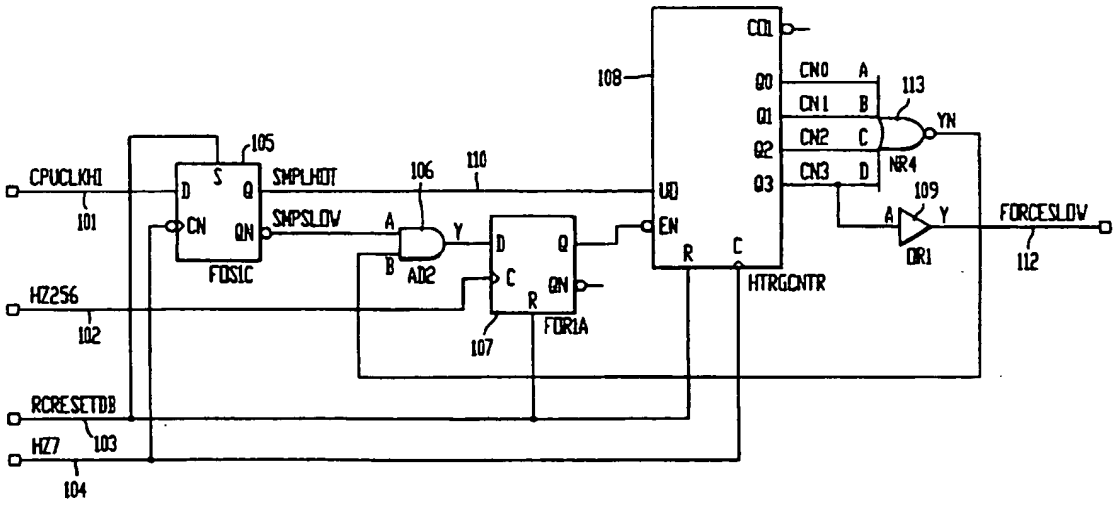

FIG. 1

EP 0 592 783 A3